

BinCAT

Purrfecting binary static analysis

June 16th 2017 - REcon

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Plan

Introduction

Demo

Under the hood

Conclusion

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Under the hood

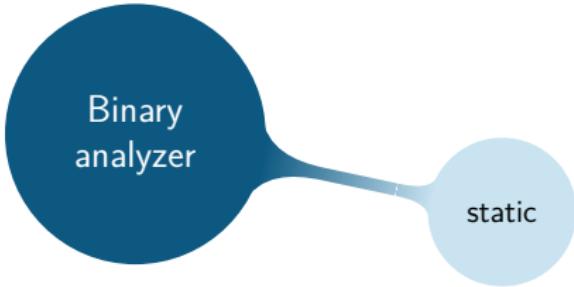
Conclusion

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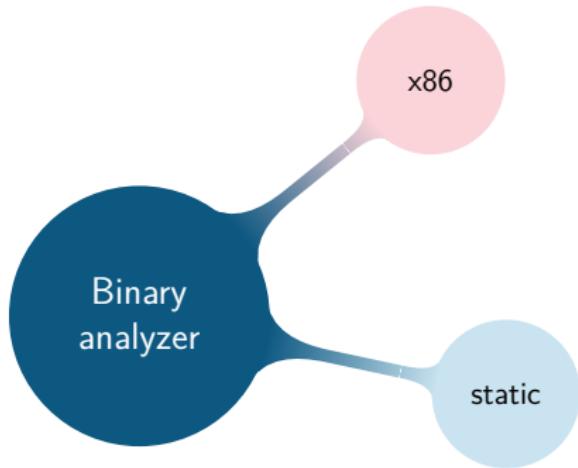


Binary
analyzer

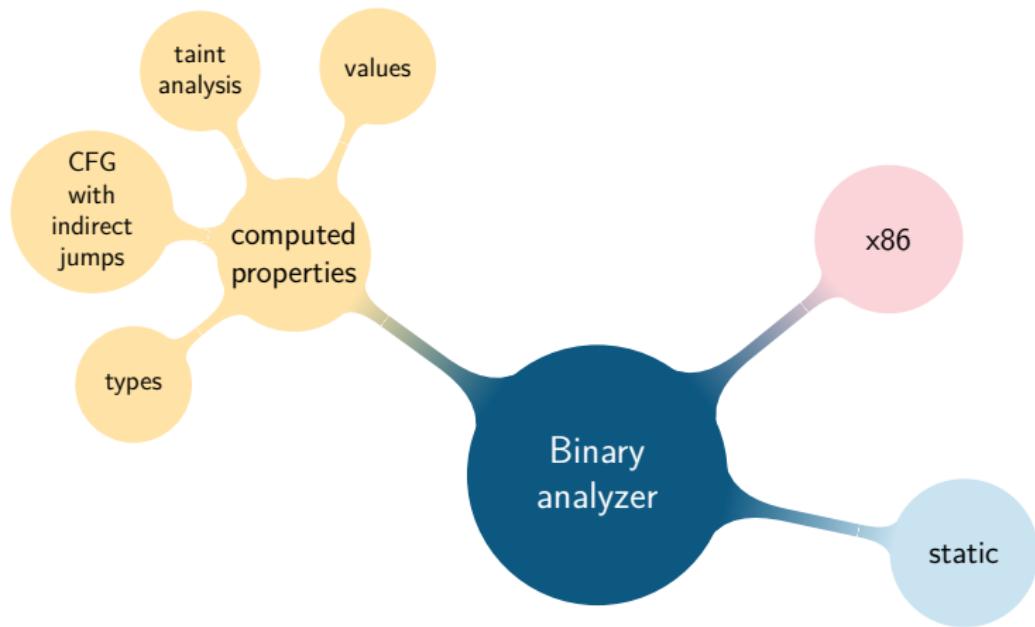
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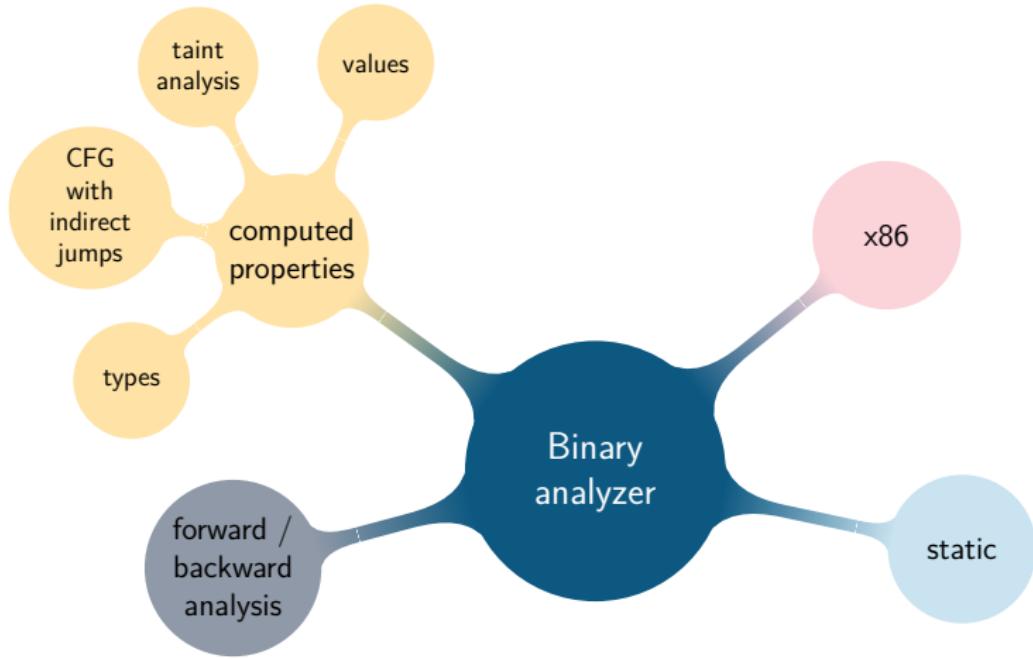
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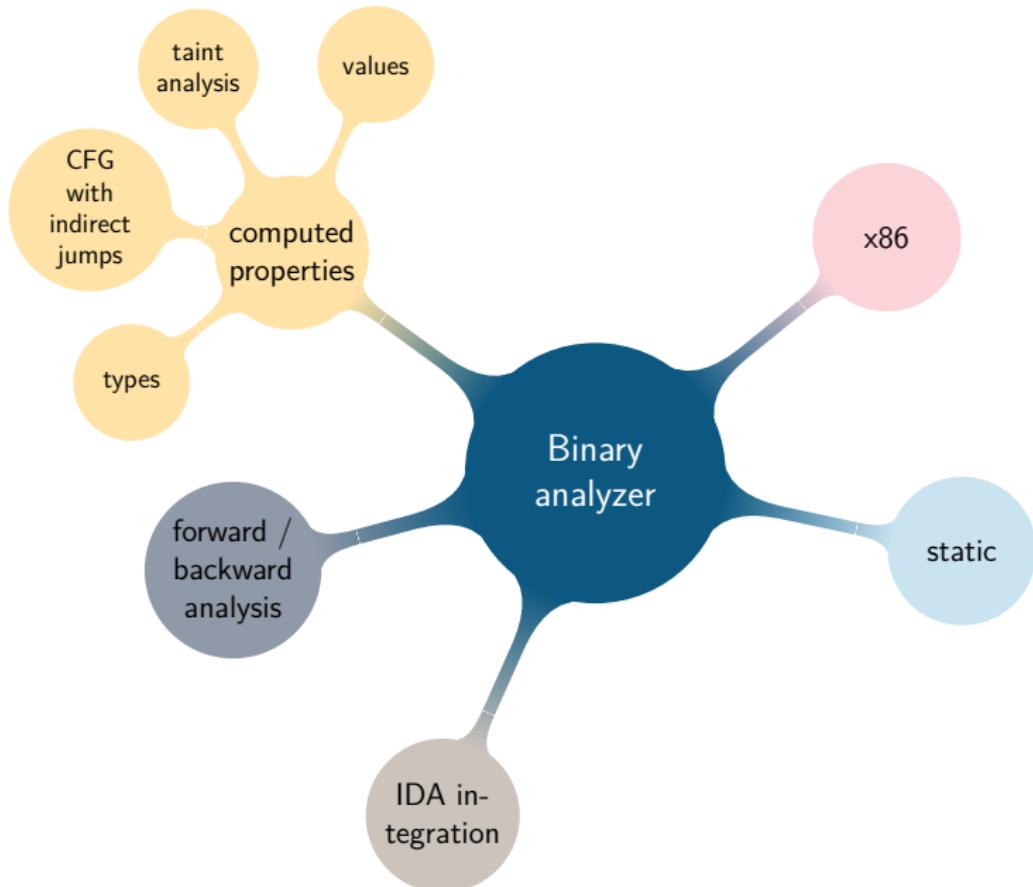
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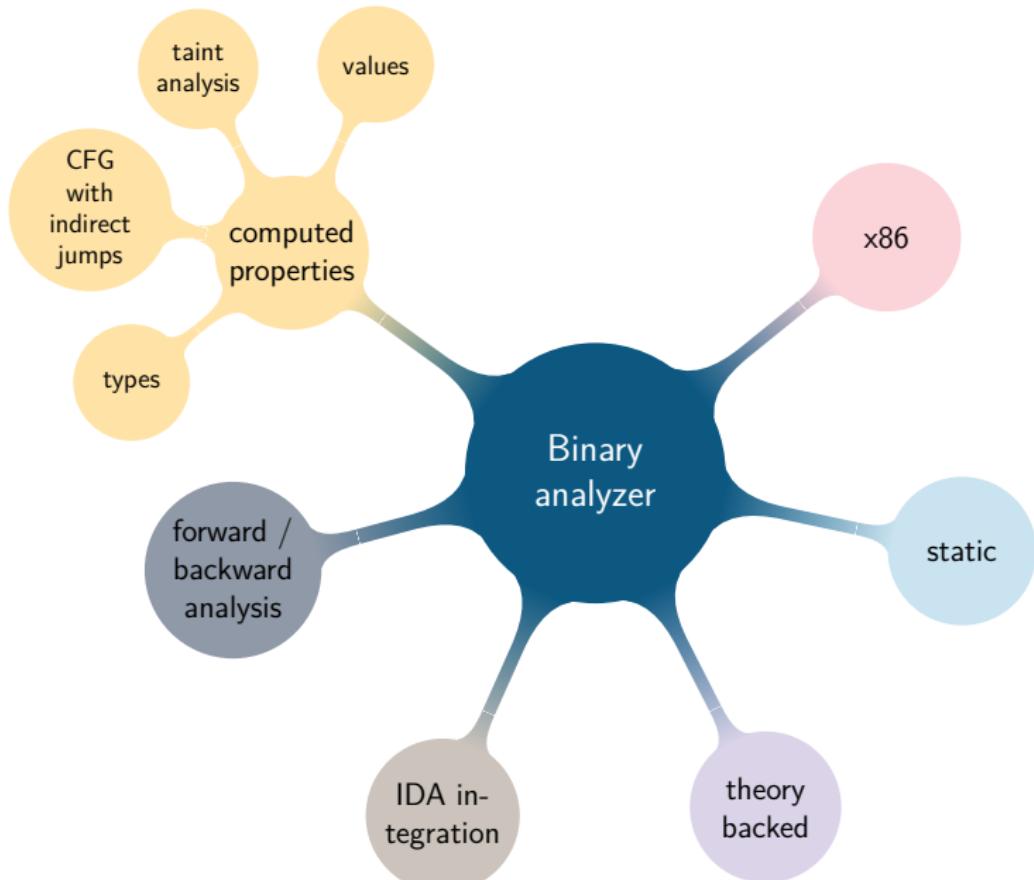
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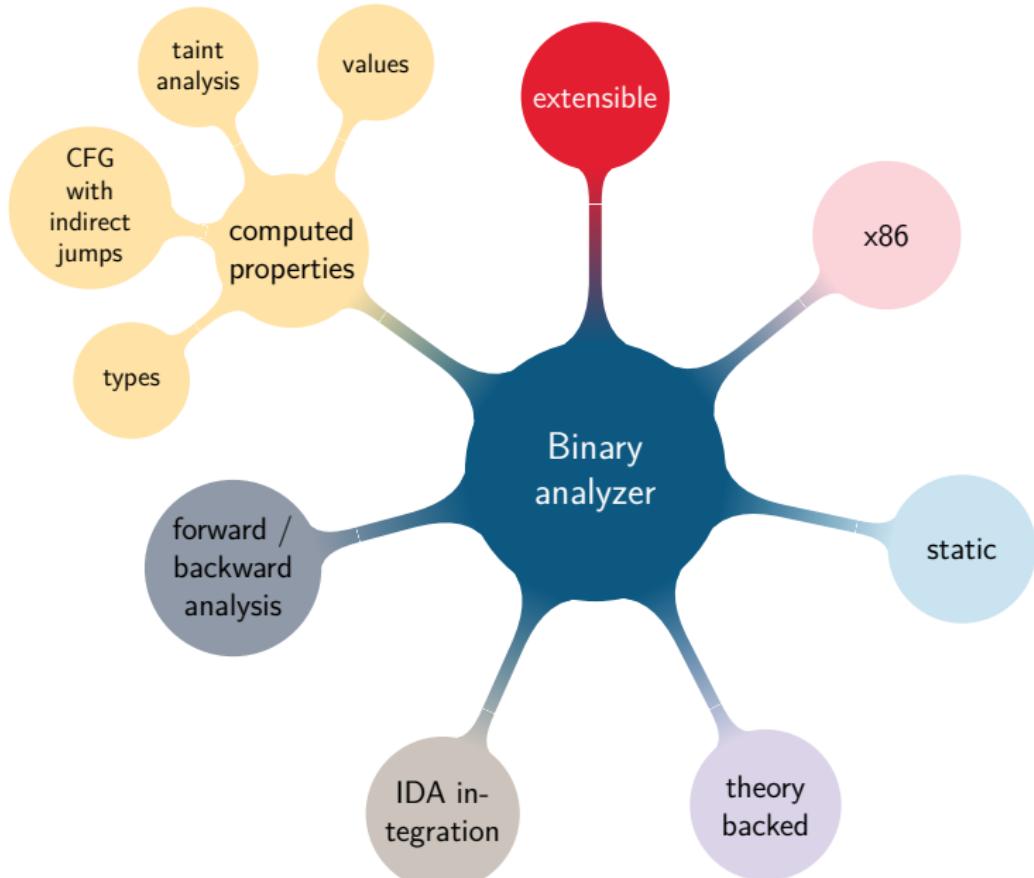
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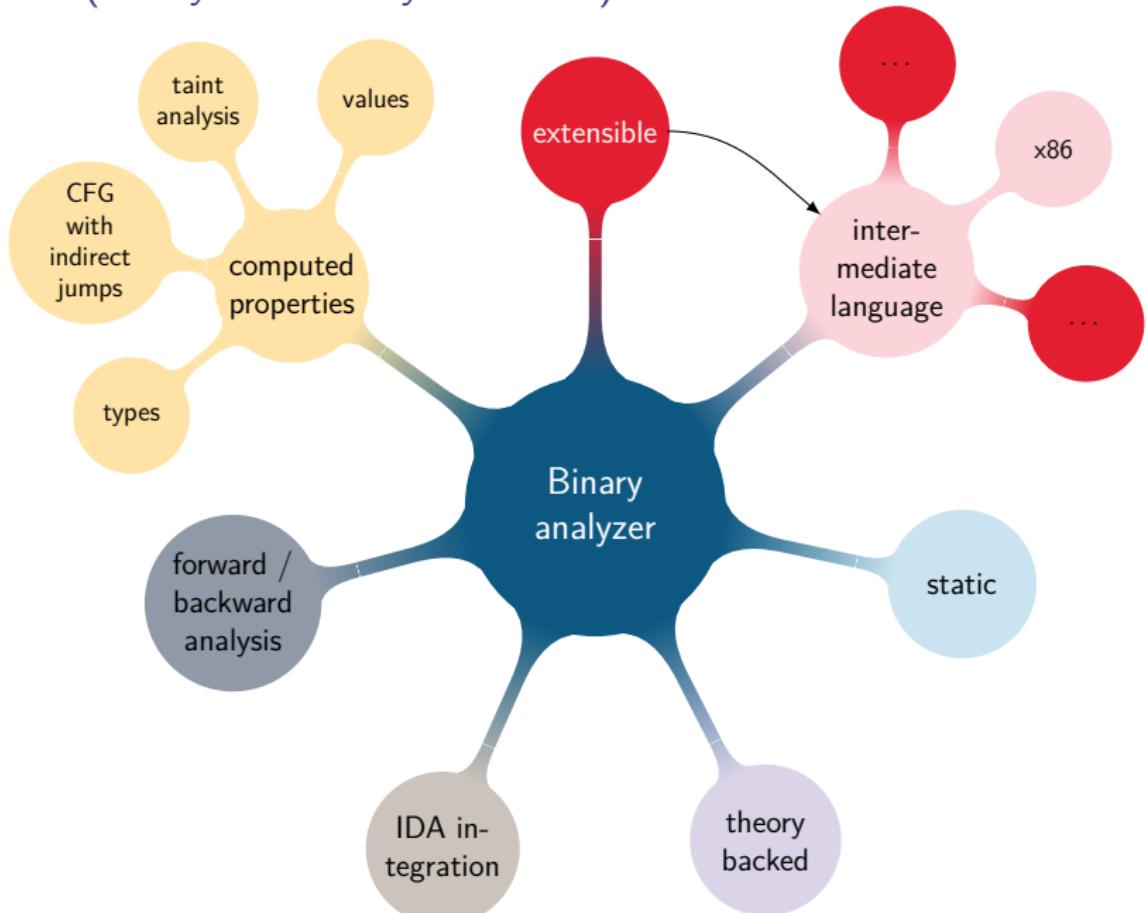
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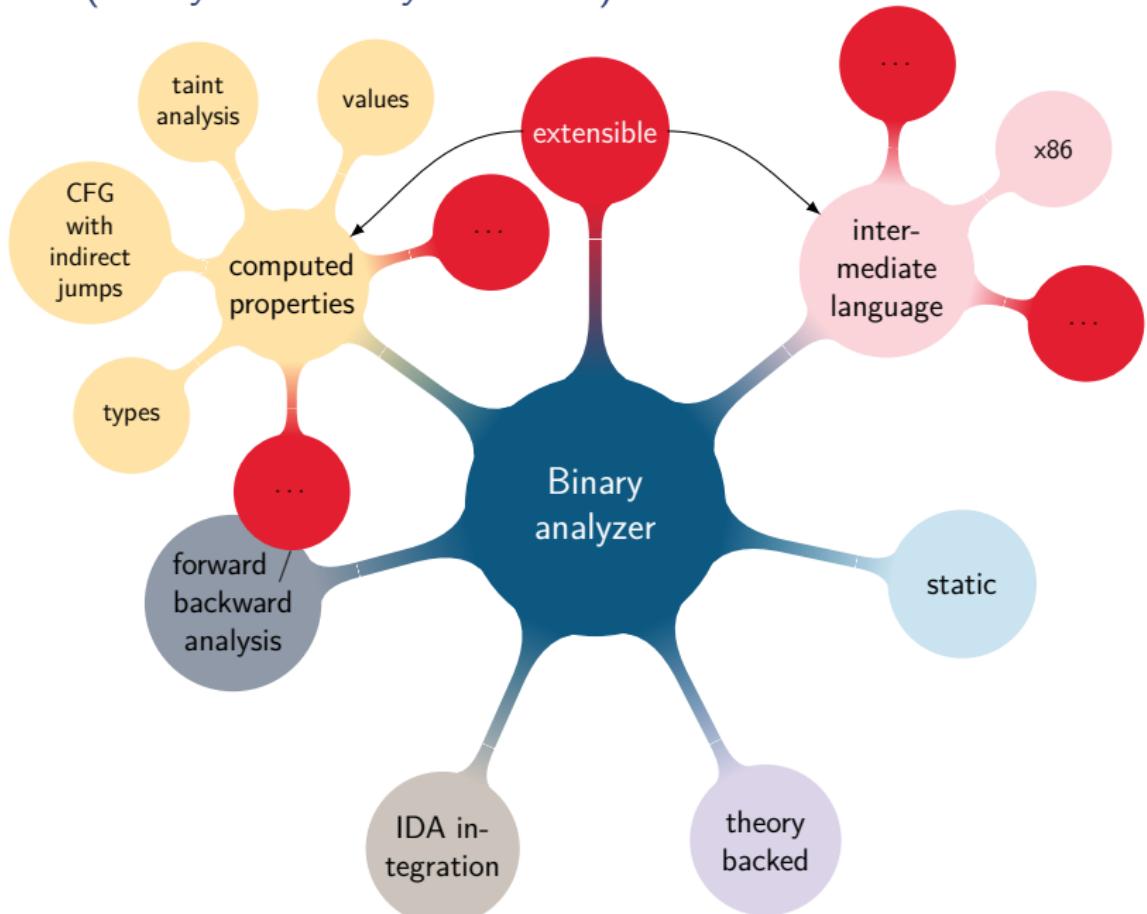
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$ ./get_key
```

```
Usage: ./get_key company department name licence
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```
$ ./get_key company department name wrong_serial  
Licence=>[025E60CB08F00A1A23F236CC78FC819CE6590DD7]  
Invalid serial wrong_serial
```

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```
$ ./get_key company department name 025E60CB0[...]
```

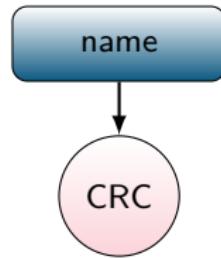
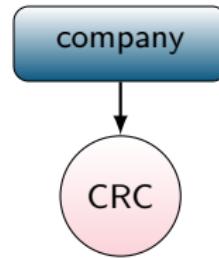
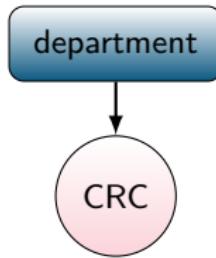
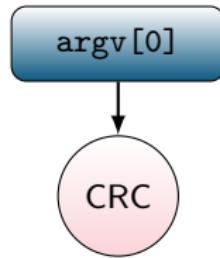
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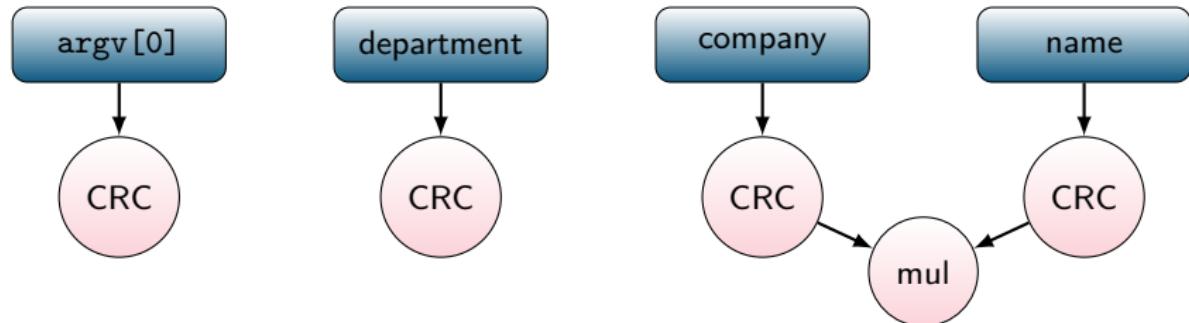
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Thank you for registering !
```

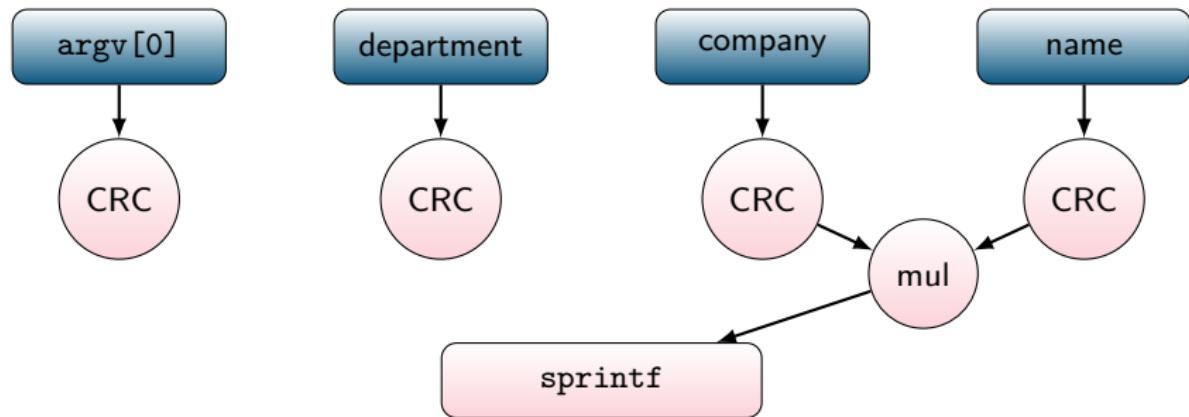
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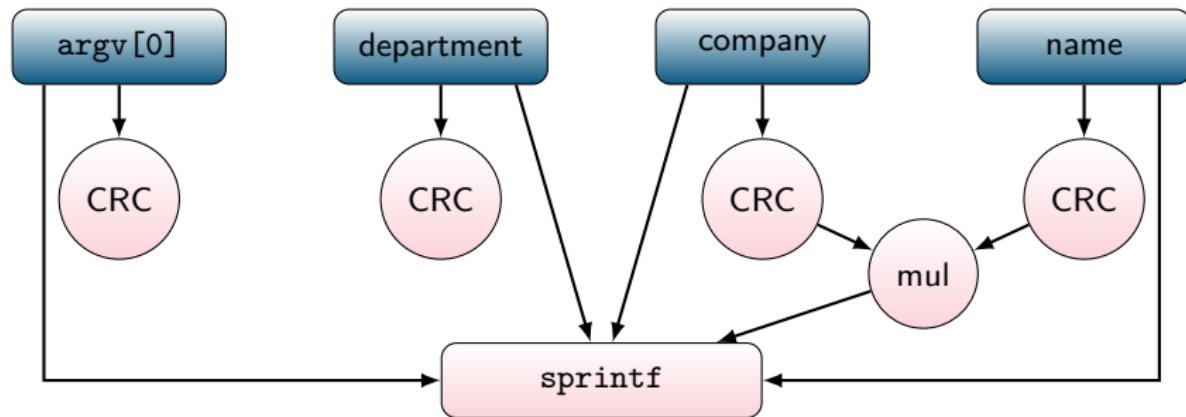
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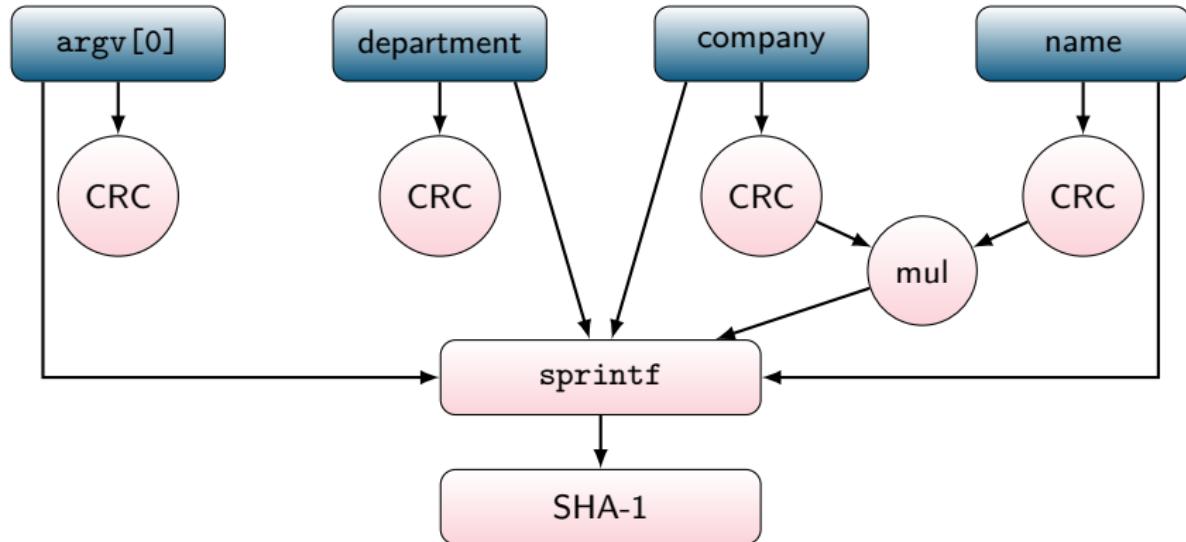
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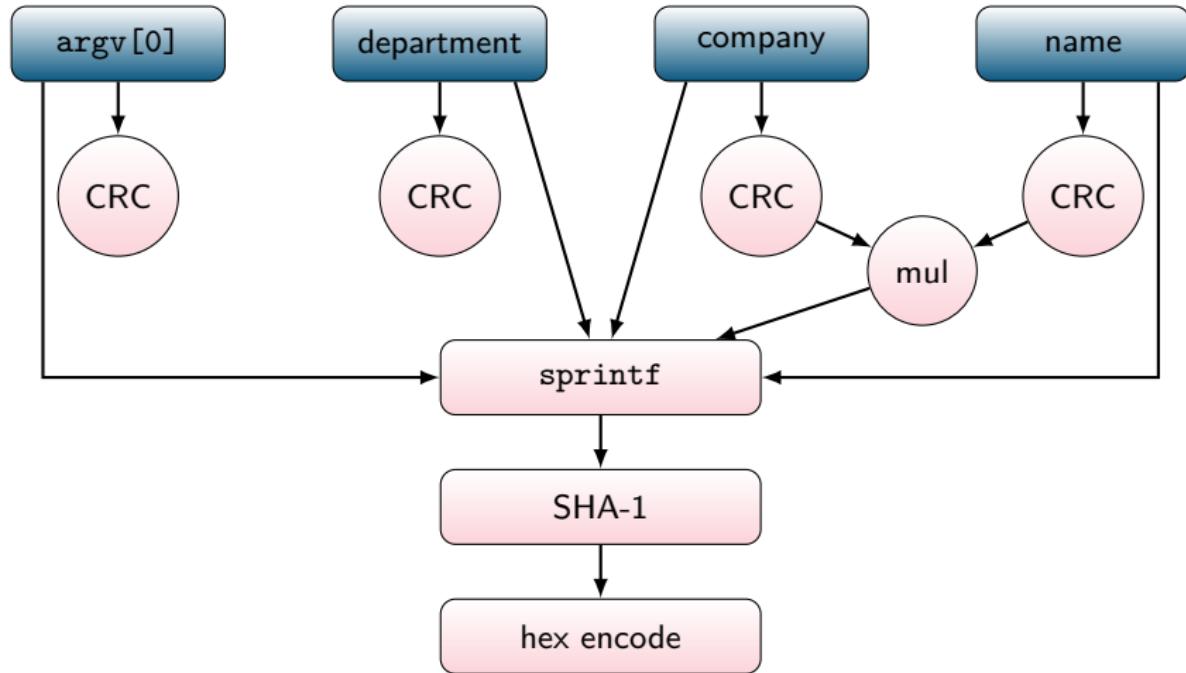
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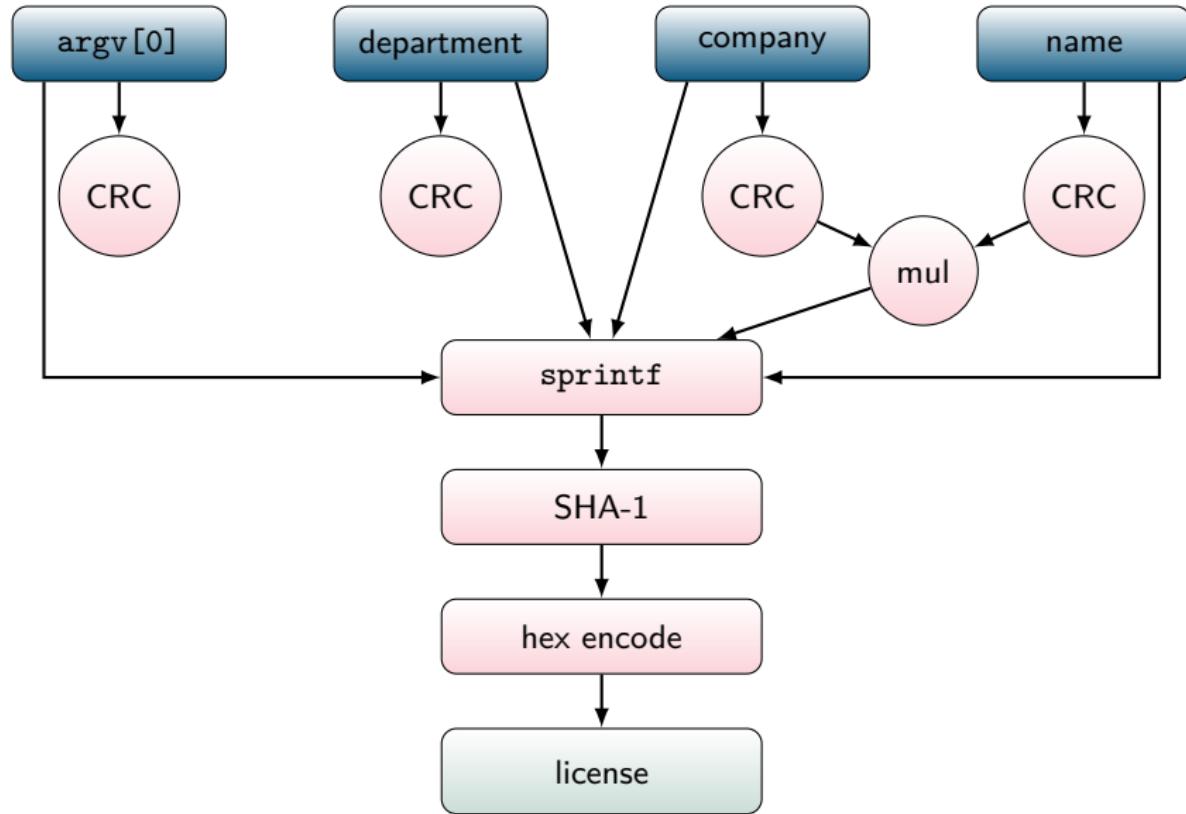
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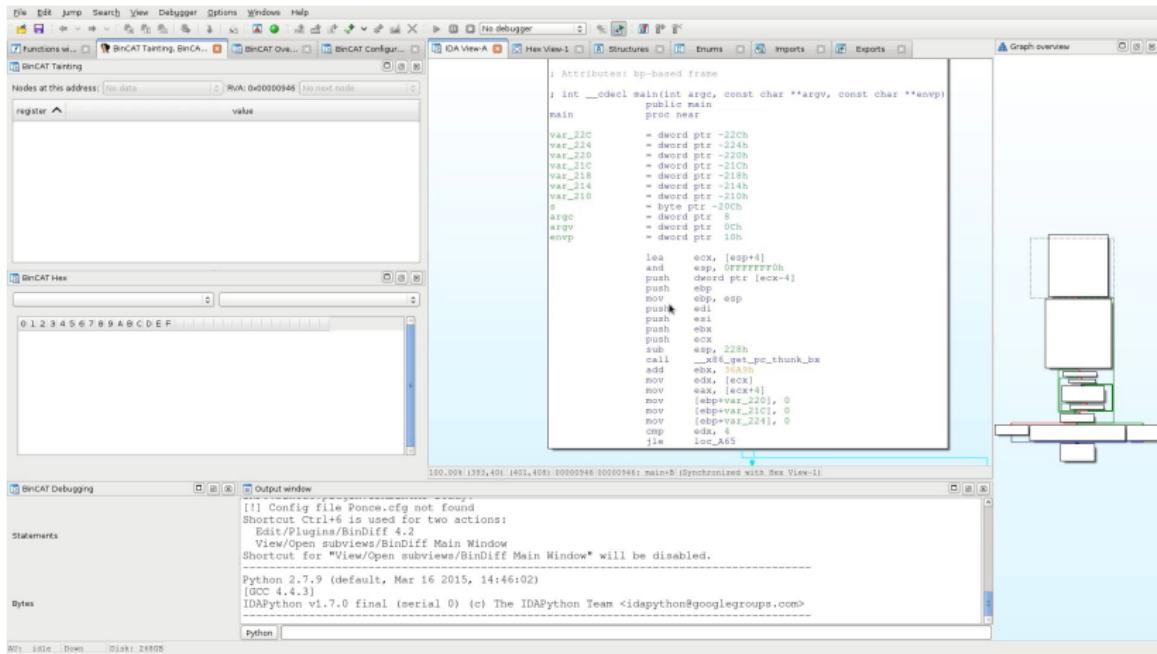
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Demo 1: BinCAT usage



Demo 2: Tainting

BinCAT Tainting

Nodes at this address: [0 other nodes] RvaA: 0x0000093b goto next node (L)

register ^	value
eax	????????
ebx	????????
ecx	????????
edx	????????
edi	????????
edx	????????
esi	????????
esp	00002000
zf	?
az	?

BinCAT Hex

global 00000100 00000128

```

0 1 2 3 4 5 6 7 8 9 A B C D E F
00000100
00000100
00000100 EE 61 4D 65 00          n a m e .
00000100
00000100
00000100
00000100
00000100
00000100 25 25 42 3B 36 32 39 36 46 32 38 39 39 30 43 46 5 5 B 8 6 2 9 6 F 2 B 9 9 0
00000100
00000100 45 44 39 31 34 45 30 37 31 45 33 37 44 33 43 36 E D 9 1 A 4 D 0 7 1 E 3 7 D 3
00000100
00000100 32 31 45 44 42 38 31 30 00 2 1 E D B 8 1 0 .
sel: [0x40, 0x47] len: 0x8

```

BinCAT Debugging

Statements: ebx <- (*esp + 0x4);

Bytes: Bd 4c 24 04

Interpreter output:

```

DEBUG:bincat:interpreter: automatic loop unrolling detection. Computed value is 0x28
DEBUG:bincat:plugin:[ANALYSIS] interpreter: set unroll parameter to its default value
DEBUG:bincat:plugin:[ANALYSIS] interpreter: at 0x04010c: library call for puts found. Looking for a stub.
DEBUG:bincat:plugin:[ANALYSIS] stubs: puts output:
DEBUG:bincat:plugin:[ANALYSIS] stubs: --- end of puts---
DEBUG:bincat:plugin:[ANALYSIS] interpreter: entered RE without previous CALL at address 00xa8a
DEBUG:bincat:plugin:[ANALYSIS] interpreter: entered interleaving mode
DEBUG:bincat:plugin:[ANALYSIS] interpreter: No new reachable states from 00xe63
DEBUG:bincat:plugin:
Python []

```

File: idle Down Disk1_21800

IOA View A

Hex View-1

Structures

Enums

Imports

Exports

Graph overview

Attributes: bp-based frame

```

int __cdecl main(int argc, const char **argv, const char **envp)
{
    main:
        proc near
            var_22C = dword ptr -22Ch
            var_224 = dword ptr -224h
            var_220 = dword ptr -21Ch
            var_21C = dword ptr -21Ch
            var_218 = dword ptr -218h
            var_214 = dword ptr -214h
            var_210 = dword ptr -210h
            s = byte ptr -200h
            argc = dword ptr 8
            argv = dword ptr 0ch
            envp = dword ptr 1ch

            lea    esp, [esp+4]
            and    esp, 0FFFFFFFh
            push   dword ptr [esp+4]
            push   ebp
            mov    ebp, esp
            push   edi
            push   esi
            push   ebx
            push   ebx
            sub    esp, 228h
            call   __x86_get_pc_thunk_bx
            add    ebx, 3A3h
            mov    edx, [BX]
            mov    eax, [BX+4]
            mov    [ebp+var_220], 0
            mov    [ebp+var_21C], 0
            mov    [ebp+var_224], 0
            cmp    edi, 0
            jle    loc_A65
}

```

The diagram illustrates the memory layout and control flow graph. It shows a stack structure with various variables (var_22C, var_224, var_220, var_21C, var_218, var_214, var_210) and pointers (s, argc, argv, envp). The stack grows downwards. A control flow graph (CFG) is shown on the right, with nodes representing basic blocks and edges representing jumps or returns. The graph includes nodes for the main function and several stubs, such as __x86_get_pc_thunk_bx and __x86_stdin.

Plan

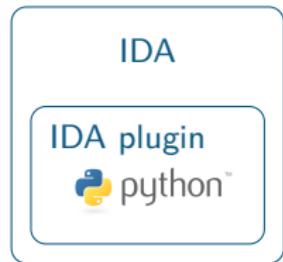
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Architecture



Architecture

IDA

IDA plugin



bincat binary

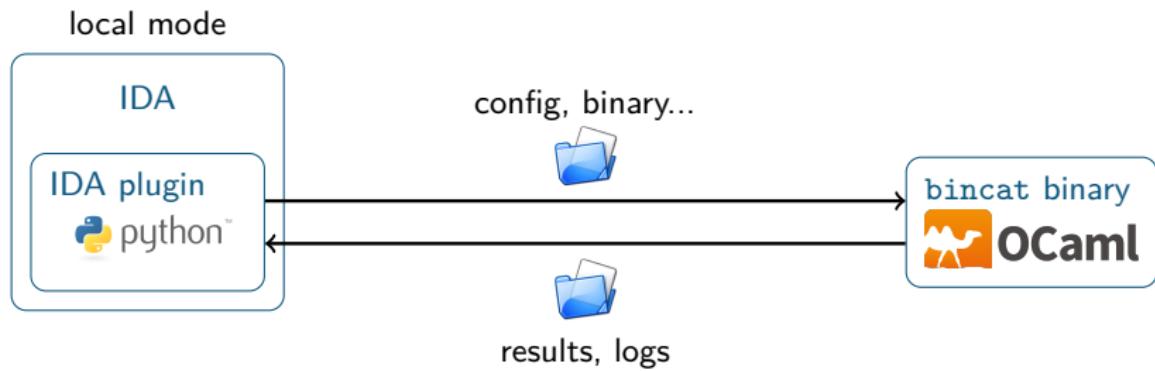


OCaml

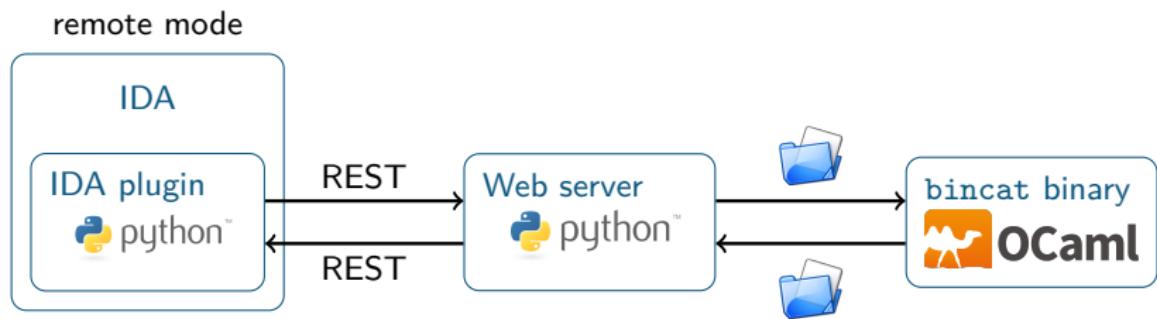
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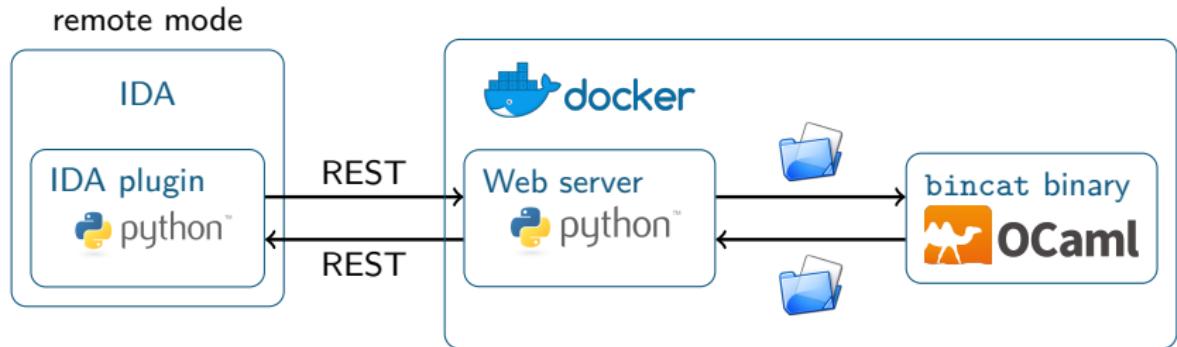
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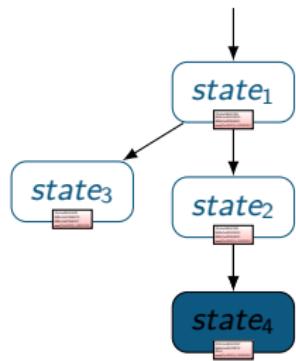
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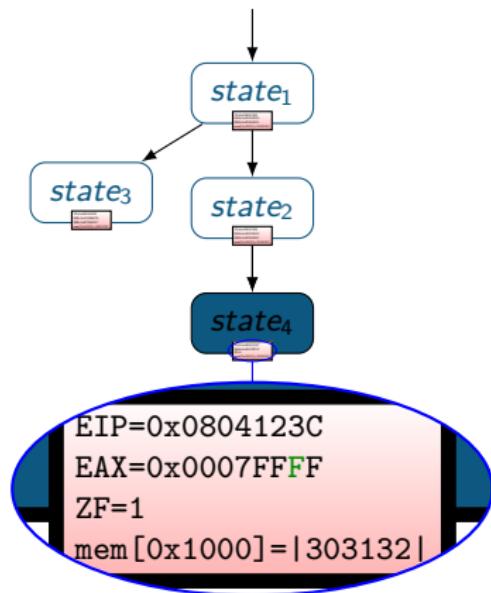
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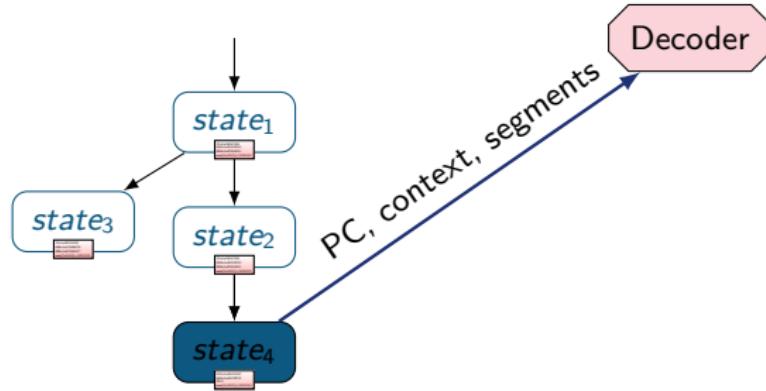
Control flow graph reconstruction



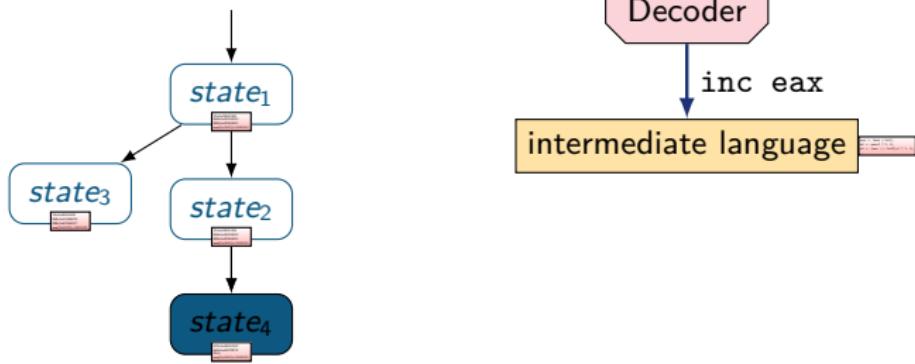
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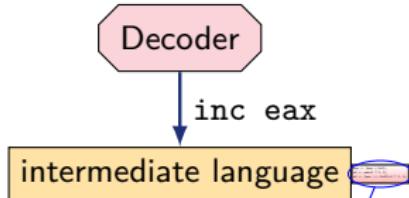
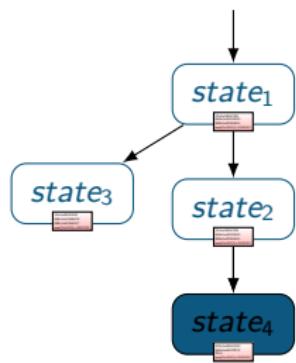
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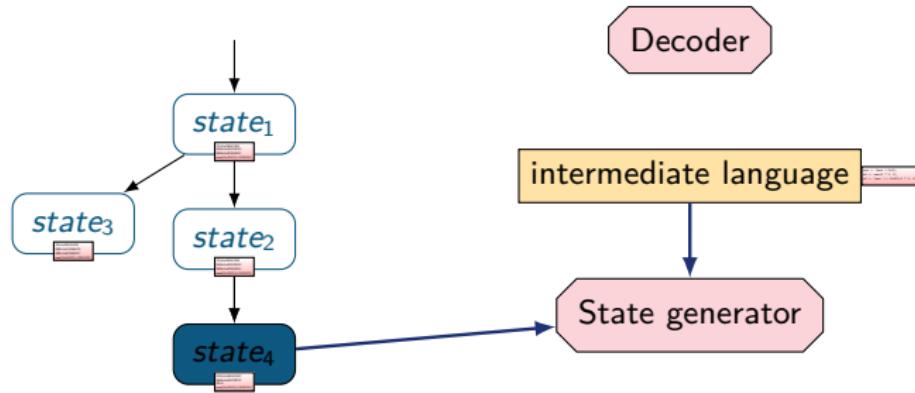


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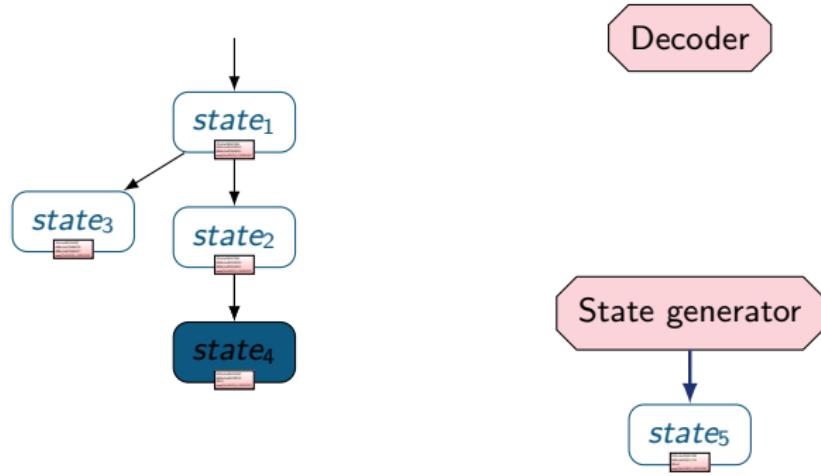


```
eax ← (eax + 0x1);
zf ← eax=0 ? 1: 0;
sf ← (eax >> 0x1f)=1 ? 1: 0;
...
```

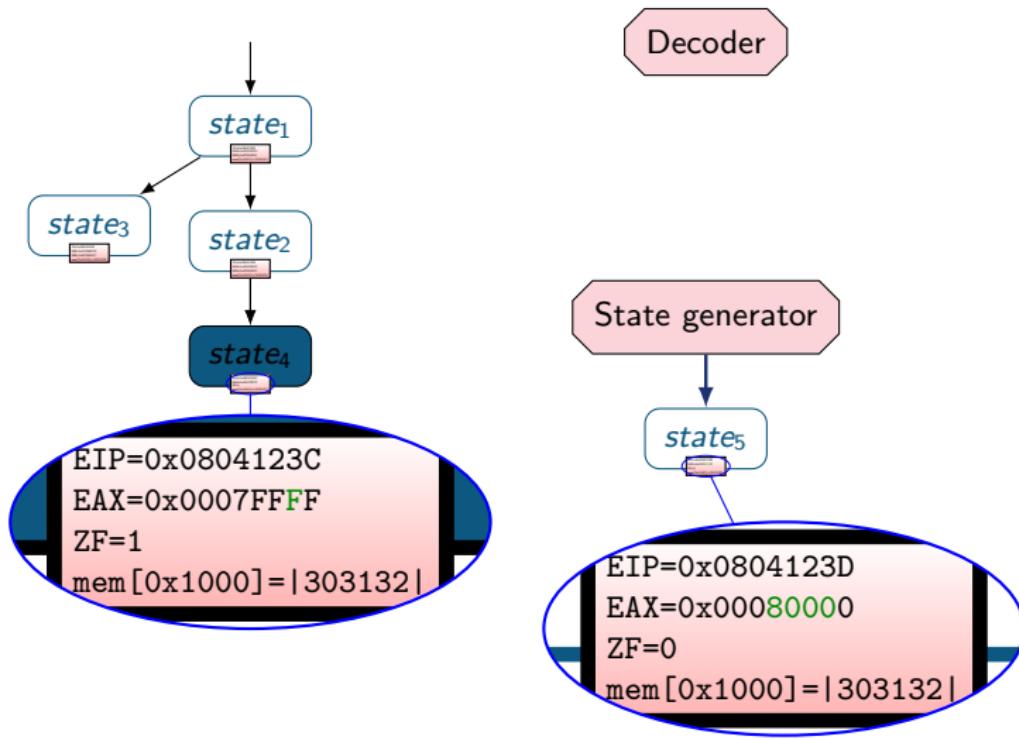
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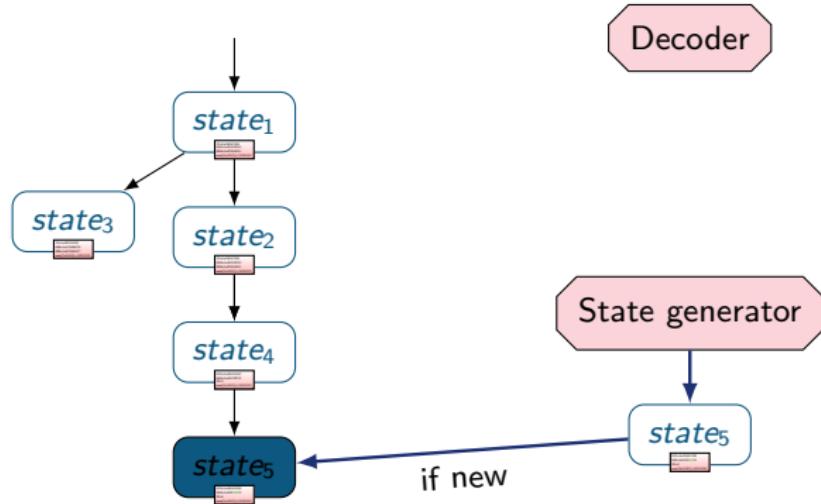
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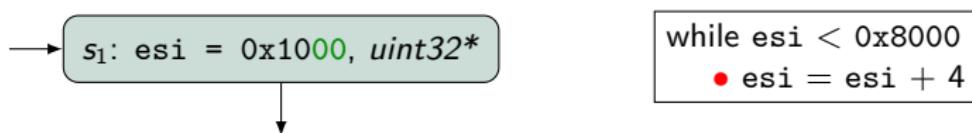


Formal correctness: static analysis by abstract interpretation

- operations on values/taint/types are done on *abstract* objects which represent sets of values/taint/types
ex: $0 \equiv \{0\}$, $? \equiv \{\text{integers}\}$, Struct $\equiv \{\text{C structs}\}$
- abstract computations are always an *overapproximation* of actual ones
- approximation example: loop widening (∇)

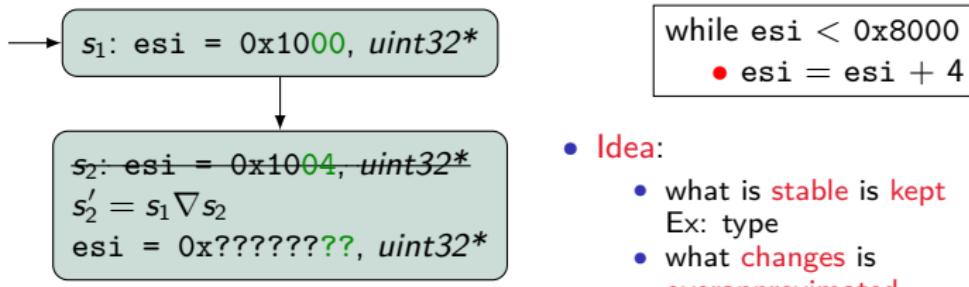
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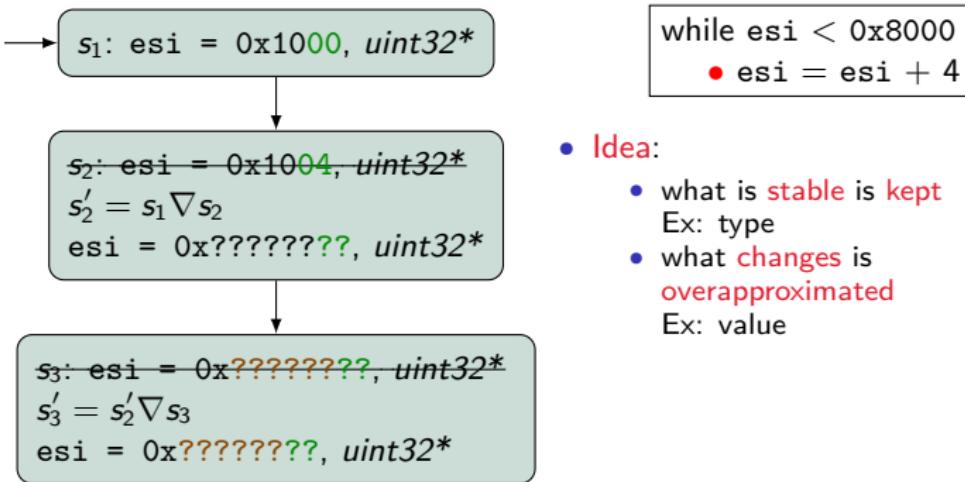


- Idea:

- what is **stable** is **kept**
Ex: type
- what **changes** is **overapproximated**
Ex: value

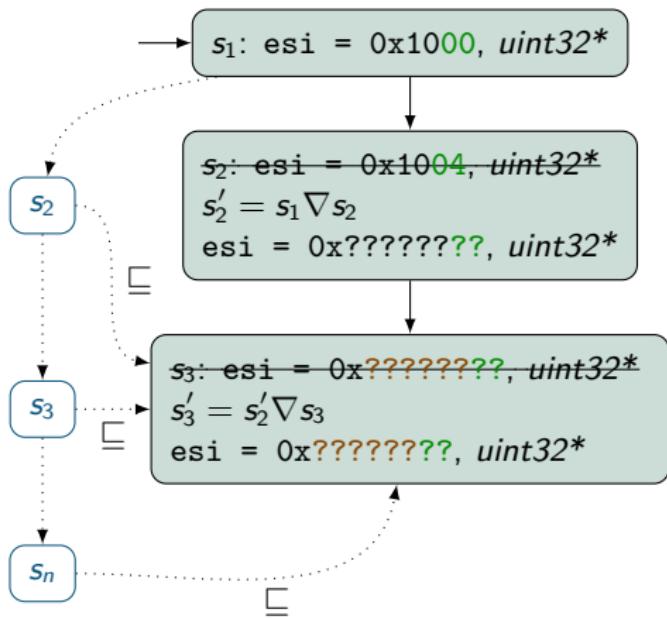
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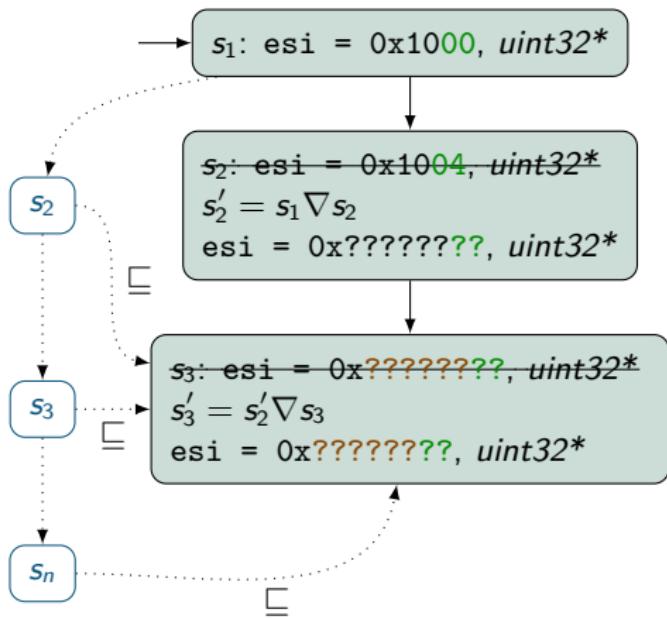


```
while esi < 0x8000
  • esi = esi + 4
```

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- Theorem 1:** (s'_i) sequence is ultimately stationary
- Theorem 2:** fixpoint s'_f is an overapproximation of the real execution trace
- some techniques allow for precision recovery

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Analyzer's performance

Example: keygenme

- 6407 instructions analyzed
- RAM usage: 90 MiB
- running time: 6s
- average: $\simeq 1060 \text{ insn/s}$

QEMU tests:

- 209 120 instructions analyzed
- RAM usage: 2.3 GiB
- running time: 23 min 30 s
- average: $\simeq 150 \text{ insn/s}$

Intel Core i7-6700K CPU @ 4,00GHz

Plan

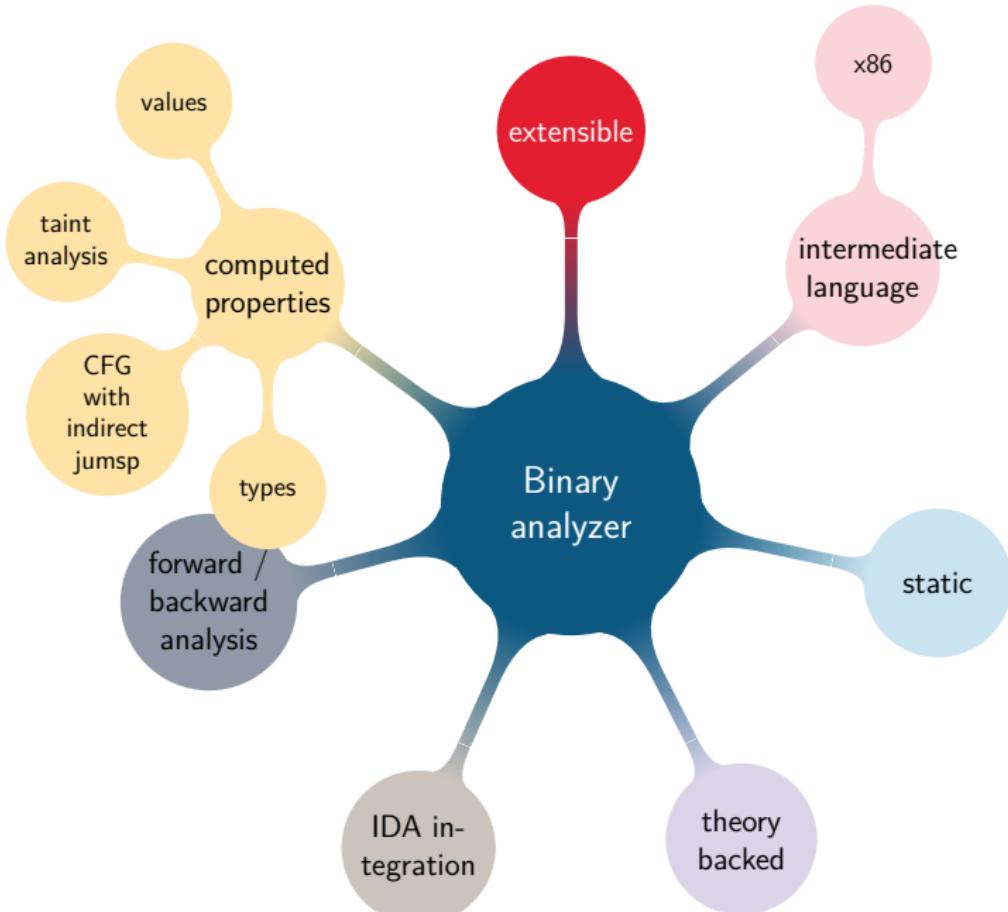
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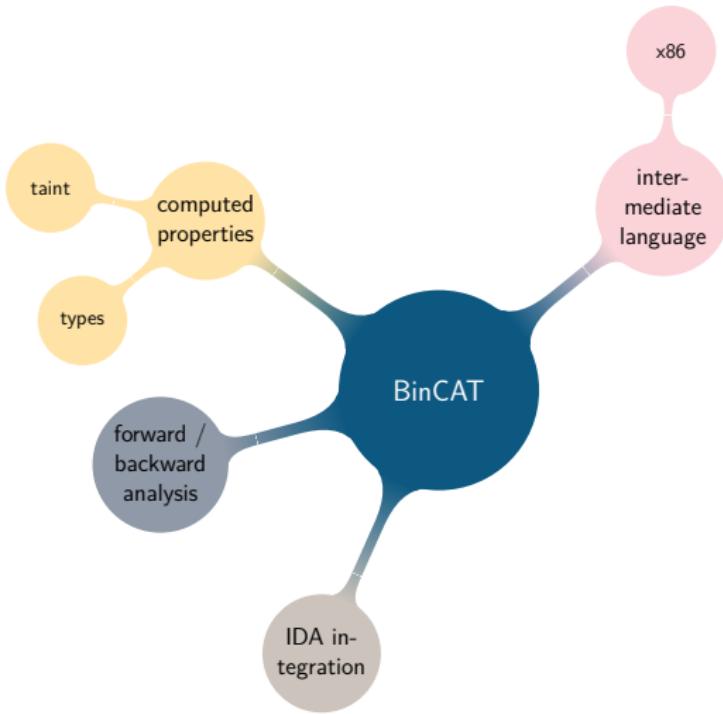
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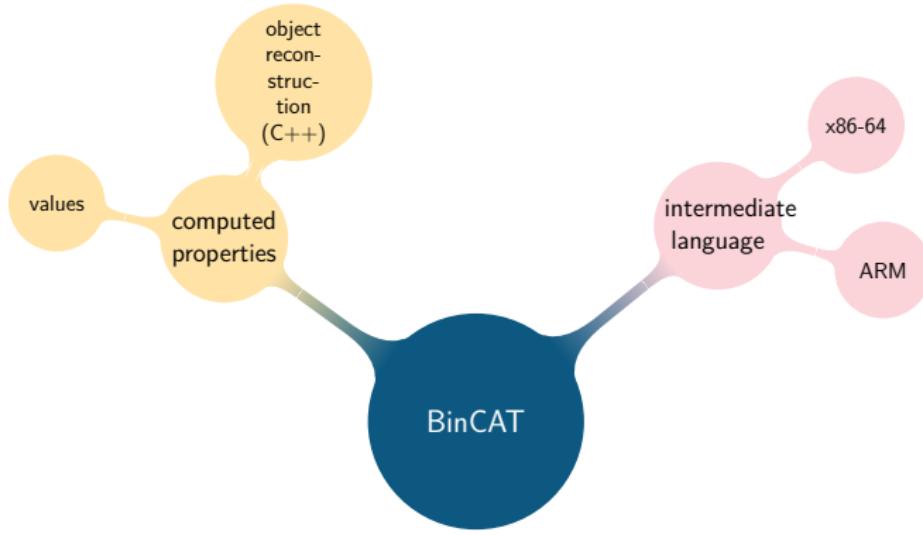


Current features improvements (planned)



- better type reconstruction
 - new types from heuristics. Ex: structures detection on stack
- several distinct taint sources
- more precise computations in backward analysis
- more standard library functions models
- type and value override in IDA
- memory definition directly in IDA

Future features



- finer approximations in values computation by using intervals
- complex objects reconstruction (C++)
- x86-64 and ARM decoders

Thanks!

Full paper (link in README):

https://www.sstic.org/media/SSTIC2017/SSTIC-actes/bincat_purrfecting_binary_static_analysis/SSTIC2017-Article-bincat_purrfecting_binary_static_analysis-biondi_rigo_zennou_mehrenberger.pdf

- project was partially financed by DGA-MI
- Get it! (AGPL licence)

<https://github.com/airbus-seclab/bincat>

`docker run -p 5000:5000 airbusseclab/bincat`

`tutorial in doc/tutorial.md`

x86 coverage

ADD	PUSH ES	POP ES	OR	PUSH CS	2 bytes
ADC	PUSH SS	POP SS	SBB	PUSH DS	POP DS
AND	ES: DAA		SUB	CS: DAS	
XOR	SS: AAA		CMP	DS: AAS	
INC			DEC		
PUSH			POP		
PUSHA	POPA	BOUND	ARPL	FS: GS:	OPSIZE: ADSIZE:
JNO	JNO	JB	JNB	JZ	JNZ
Grp1	Grp1	Grp1	TEST	XCHG	MOV
NOP	XCHG	EAX	CWD	CDQ	CALL
MOV	EAX	MOVS	CMPS	TEST	STOS
M	O	N	Y	INT3	INT
SHIFT	RETN	LES	LDS	MOV	ENTER LEAVE RETF INT INTO RETD
Grp2	AAM	AAD	SALC	XLAT	FPU
LOOPNZ	LOOPZ	LOOP	JCXZ	IN OUT	CALL JMP JMPF JMPS IN OUT
LOCK:	INT1	REPNE	REP	HLT CMC	Grp3 CLC STC CLI STI CLD STD Grp4 Grp5

x86 coverage - Second table

Grp6	Grp7	LAR	LSL		CLTS		INVD	WBINVD		UD2		NOP				
SSE	SSE	SSE	SSE	Prefetch SSE1	HINT	NOP										
MOV CR DR					SSE		SSE	SSE	SSE	SSE	SSE	SSE				
WRMSR	RDTSC	RDMSR	RDPMC	SYSENTER	SYSEXIT		GETSEC SWX	MOVBE		SSE						
CMOV	CMOV	CMOV	CMOV													
SSE	SSE	SSE	SSE													
MMX	MMX	MMX	MMX													
MMX SSE VMX																
JNO	JNO	JB	JNB	JZ	JNZ	JBE	JA	JS	JNS	JP	JNP	JL	JNL	JLE	JNLE	
SETNO	SETNO	SETB	SETB	SETNB	SETZ	SETNZ	SETBE	SETA	SETS	SETNS	SETP	SETNP	SETL	SETNL	SETLE	SETNLE
PUSH FS	POP FS	CPUID	BT	SHLD			PUSH GS	POP GS	RSM	BTS	SHRD	FENCE	IMUL			
CMPXCHG	LSS	BTR	LFS	LGS	MOVZX		POPONT	UD	BTx	BTC	BSF	BSR	MOVSX			
XADD	SSE	SSE	CMPXCHG		BSWAP											
MMX	MMX	MMX	MMX		SSE		SSE	SSE	SSE	SSE	SSE	SSE	SSE			
MMX	MMX	MMX	MMX		SSE		SSE	SSE	SSE	SSE	SSE	SSE	SSE			
MMX	MMX	MMX	MMX		SSE		SSE	SSE	SSE	SSE	SSE	SSE	SSE			

Currently implemented lattices

